

Appl. No. 10/605,094  
Amdt. dated May 08, 2006  
Reply to Office action of March 03, 2006

**Amendments to the Drawings:**

As required by the Examiner, applicant has produced replacement drawings for Figures 1-5. Drawings are labeled by the legend "Prior Art" to indicate that the drawings are based on a previous invention and known to one skilled in the art. Please refer to the attached drawings  
5 for further detail.

Attachment: Replacement Sheet

5 page(s)

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### **REMARKS**

**Figures 1-5 should be designated by a legend such as –Prior Art– because only that which is old is illustrated**

Replacement sheets are included for Figures 1-5 being labeled by the legend “Prior Art”  
5 as requested by the Examiner. No new matter is entered.

### **Objections to the Specification**

Various typographical errors in the specification have been corrected in accordance to Examiner remarks and suggestions. Please refer to the “amendments to the  
10 specification” section above for specific details about corrections and modifications made. Changes made to the specification only reflect corrections in spelling and/or grammar, with no new subject matter introduced, nor current subject matter or meaning being altered.

15 **Rejection of Claim 1 under 35 U.S.C 103(a) as being unpatentable over Chu (US 6,459,665) in view of Nakano et al (US 5,742,568)**

Although Chu teaches a compensator circuit including: a phase-lead compensator, a phase-lag compensator, a band pass filter and an adder, and Nakano et al teach a phase compensation circuit, applicant asserts that it is not obvious to remove the phase-lag  
20 compensator in the invention of Chu by applying the teachings of Nakano and arrive at the present invention. Applicant asserts that Nakano does not in fact consider a case of phase lag compensation; hence Nakano does not provide phase-lag compensator and therefore cannot teach the removal of such.

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The Examiner has suggested that Nakano teaches a compensator circuit not comprising any phase-lag compensator, and has provided (Col 9 line 66 – Col 10 line 10) as a reference which states "...the phase compensation filter may be constituted by using three or more first-order phase lead filters or using phase lead filters". However, this  
5 reference merely details the composition of a compensator circuit, and does not teach removal of a phase-lag compensator.

Applicant firstly asserts that Nakano in fact cannot teach removal of a phase-lag compensator, because such a component is not utilized in the teachings of Nakano. Nakano states "a phase lag compensation filter...may be added to the circuit" (Col 8  
10 lines 1-8) implying that no such component is used in the examples provided. Nakano states further that "the characteristics of the phase compensation circuit 10 will be examined... Here, it is assumed that no phase lag compensation is performed. Thus only a phase lead compensation filter will be described hereunder." (Col 8 lines 64-67). Therefore, subsequent referral to the phase compensation circuit 10, more specifically  
15 refers only to the phase lead compensation filter. Inspection of Figs 1, 11 and 12 will further confirm that only phase compensation circuit 10 (being a phase lead compensation filter from the above description) is used because the phase-lag compensation is assumed not to be performed.

Furthermore, applicant asserts that Nakano assumes specific system and operating  
20 conditions in order to validate the exclusion of a phase-lag compensator. Nakano assumes "the system has characteristics in which the phase lag due to the delay time abruptly increases as the frequency becomes higher" (Col 9 lines 15-17) and "in the case of this system, the phase lead thereof should be at least 100 degrees or so" (Col 9 lines 10-12). Therefore, using these assumptions, trackability of the system is only accurate for higher  
25 frequencies when phase lag increases. Applicant asserts that this does not ensure stability at lower frequencies as Nakano does not detail an operating condition at low frequency. This in contrast to the present invention, where the compensator circuit 56 comprises a

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band pass filter 64 with transfer function shown in Fig.7 to provide low frequency gain and ensure stability and tracking accuracy (see paragraphs 26-28). Applicant asserts that the omission of the phase-lag compensator as taught by Nakano is only valid under certain specific conditions, and does not ensure system stability under all practical  
5 operating conditions.

Secondly, Applicant asserts that it would not have been obvious to remove the phase-lag compensator from the invention of Chu because Chu teaches against the removal of a phase-lag compensator. Specifically, Chu teaches that the lag compensator is one of the components utilized to lower the steady state error within the error signal. For  
10 example, Chu states "the lag compensator and the bandpass filter 34 is capable of compensating the error signal at high-speed rotating frequency in an optical storage device. Hence, the steady state error within the error signal is lowered." (Col 4 lines 41-45) and "The summation signal from the lag compensator 32' and the bandpass filter 34' is capable of compensating the high-speed rotating frequency so that steady state error  
15 within the error signal is lowered" (Col 5 lines 8-12). Therefore, the lag compensator and bandpass filter are used in conjunction to form a summation signal, which in turn is used to reduce steady state error of the error signal. Due to this configuration, applicant asserts that there would be no motivation to remove the phase-lag compensator in the circuit of Chu, as removal of the phase-lag compensator would inadvertently affect the function of  
20 reducing steady state error.

In summary, applicant asserts that it is not obvious to remove the phase-lag compensator of Chu through the teachings of Nakano because Nakano does not include or explicitly teach the removal of such a component. Nakano simply omits the inclusion of a phase-lag compensator because he only considers an isolated case where the phase lag  
25 increases as the frequency becomes higher. Furthermore, Nakano does not teach how to cope with alternative cases including low frequencies. Applicant also asserts that there would be no motivation to remove the phase-lag compensator of Chu, as Chu teaches it is

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required for reduction of steady state error of the error signal. For at least the above mentioned reasons, applicant respectfully requests that the Examiner re-evaluate Claim 1 for consideration of its allowance in light of the above.

5 **Rejection of Claims 2,3 under 35 U.S.C 103(a) as being unpatentable over Chu (US 6,459,665) in view of Nakano et al (US 5,742,568)**

Applicant points out that Claims 2,3 are dependant upon base Claim 1. Should an allowance be made for Claim 1, applicant asserts that Claims 2,3 should be found allowable as having a dependency upon Claim 1.

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**Rejection of Claims 4-8 under 35 U.S.C 103(a) as being unpatentable over Chu (US 6,459,665) in view of Nakano et al (US 5,742,568)**

Applicant points out that Claims 4-8 are dependant upon intervening Claim 3, which is in turn dependant upon independent Claim 1. Should an allowance be made for Claim 1,  
15 applicant asserts that Claims 3 should be found allowable, which in turn should call for an allowance on dependent Claims 4-8.

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**Rejection of Claim 9 under 35 U.S.C 103(a) as being unpatentable over Chu (US 6,459,665) in view of Nakano et al (US 5,742,568)**

Regarding Claim 9, applicant points out that Claim 9 is a method claim analogous to the device claim presented in Claim 1. Please refer to remarks made for Claim 1 for further details with regard to Claim 9.

In particular, applicant asserts that it is not obvious to remove the phase-lag compensator from the invention of Chu as taught by Nakano et al. Applicant asserts that  
25 Nakano does not teach initially having a phase-lag compensator and hence cannot teach its removal. Furthermore, Chu teaches against the removal of the phase-lag compensator as it is required for reduction of steady state error of the error signal. Further details can

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be found in the remarks section for Claim 1.

For at least the above described reasons, applicant asserts that Claim 9 should be  
found allowable over the teachings of Chu and Nakano, and respectfully requests the  
5 Examiner re-evaluate Claim 9 for its allowance.

Sincerely yours,



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is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)